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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,751	07/28/2003	Kun-Hong Chen	LEE0015-US	4408

7590 12/15/2004

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,751	CHEN, KUN-HONG	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/28/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement filed on July 28th, 2003 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

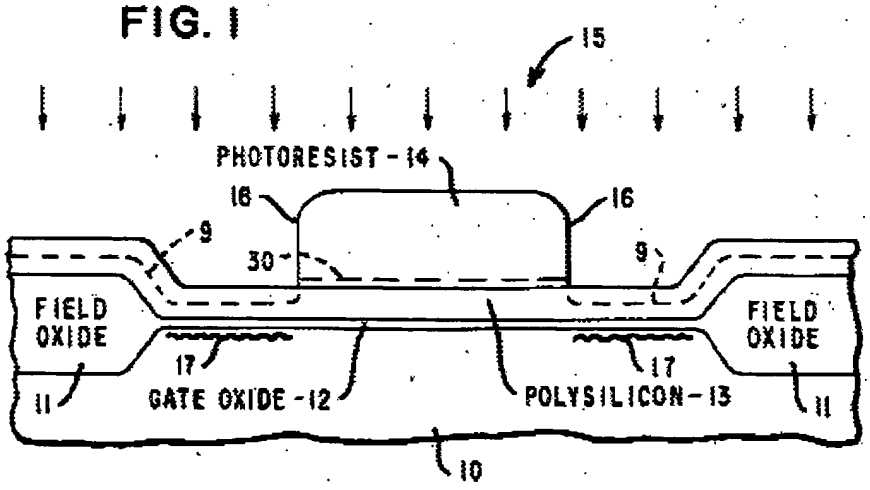
A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Miller et al. (U.S. Patent 4,682,404).

In re claim 1, **Miller** discloses a method of forming a lightly doped drain comprising: providing a semiconductor structure **10**; forming an insulating layer **12** on the semiconductor structure; forming a conductive layer **13** on said insulating layer; forming a photo resist layer **14**, having a transferred pattern, on the conductive layer (col. 5, lines 36-53 and FIG. 1);

FIG. 1

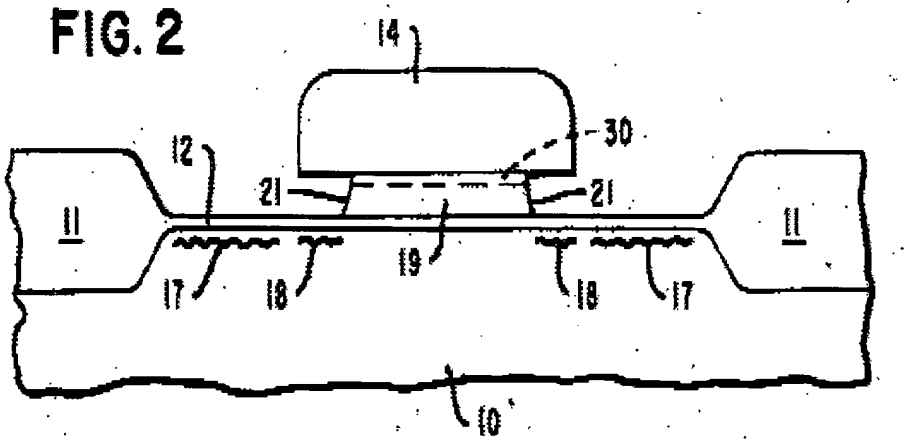


removing a portion of the conductive layer to expose a portion of the insulating layer, the step of removing uses the photo resist layer as a first mask (col. 5, lines 54-65);

implanting multiple (M) first ions **15** into the semiconductor structure, the step of implanting uses the photo resist layer and the conductive layer as a second mask (col. 5, lines 66 to col. col. 6, line 19 and FIG. 1);

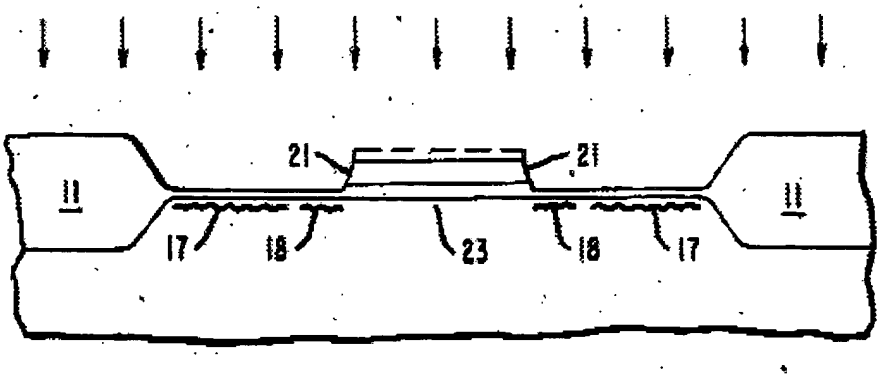
isotropic etching a portion of the conductive layer such that undercut of the conductive layer under the photo resist layer is observed (col. 6, lines 20-44 and FIG. 2); and

FIG. 2



implanting multiple (M) second ions into the semiconductor structure to form the lightly doped drain **18**, the step of implanting uses the undercut conductive layer as a third mask (col. 6, lines 45-64 and FIG. 3).

FIG. 3



In re claim 6, **Miller** discloses that the step of removing a portion of the conductive layer **13** comprises dry etching a portion of the conductive layer (col. 6, lines 20-44).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

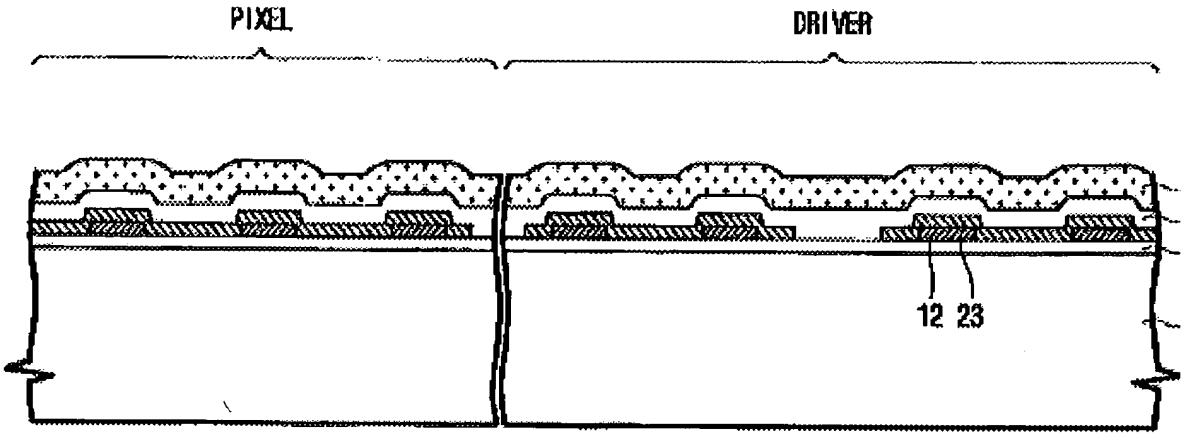
3. Claims 8-11 are rejected under 35 U.S.C. 102(e) as being anticipated by You (U.S. Patent 6,806,036).

In re claim 8, **You** discloses a method of forming a lightly doped drain, the lightly doped drain is formed in a thin film transistor, comprising:

providing a glass substrate **10** and a polysilicon structure **13** on the glass substrate; depositing an insulating layer **15** on the polysilicon structure and the glass

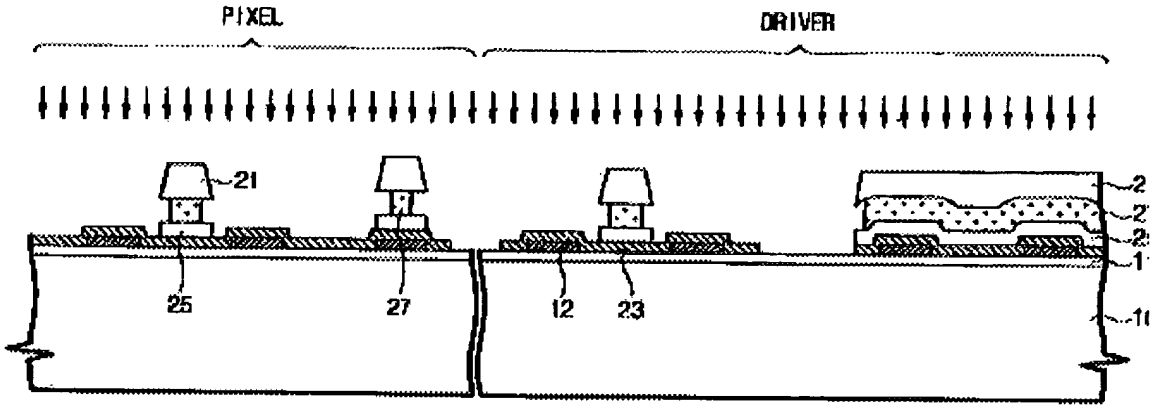
substrate; depositing a metal layer **17** on the insulating layer (col. 3, lines 34-64 and FIG. 2);

Fig. 2



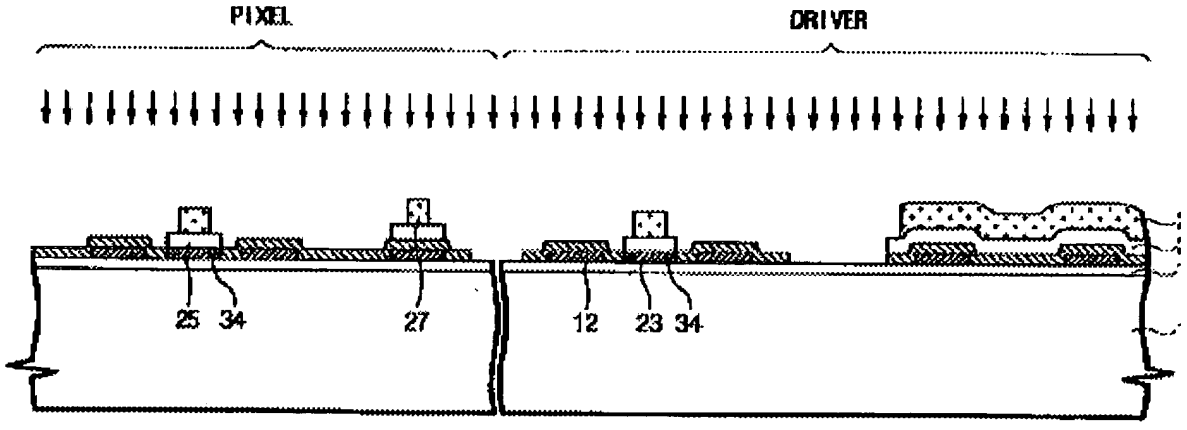
forming a photo resist layer **21**, having a transferred, pattern on the metal layer; dry etching a portion of the metal layer to expose a portion of the insulating layer, the step of dry etching uses the photo resist layer as a first mask; implanting multiple (M) first ions into the polysilicon structure, the step of implanting uses the photo resist layer and the metal layer as a second mask; isotropic etching a portion of the metal layer such that undercut of the metal layer under the photo resist layer is observed (col. 3, line 65 to col. 4, line 29 and FIG. 4);

Fig. 4



removing the photo resist layer; and implanting multiple (M) second ions into the polysilicon structure to form the lightly doped drain **34**, the step of implanting uses the undercut metal layer as a third mask (col. 4, line 61 to col. 5, line .13 and FIG. 5).

Fig. 5



In re claim 9, **You** discloses that the step of isotropic etching comprises wet etching a portion of the metal layer (col.3, line 65 to col. 4, line 8).

In re claim 10; **You** discloses a method of forming a lightly doped drain comprising: providing a semiconductor structure, the semiconductor structure including a substrate **10** and a polysilicon structure **13** on the substrate; forming an insulating layer **15** on the semiconductor structure; forming a conductive layer **17** on the insulating layer (col. 3, lines 34-64 and FIG. 2); forming a photo resist layer **21**, having a transferred, pattern on the conductive layer; removing a portion of the conductive layer to expose a portion of the insulating layer, the step of removing uses the photo resist layer as a first mask; implanting multiple (M) first ions into the polysilicon structure, the step of implanting uses the photo resist layer and the conductive layer as a second mask; isotropic etching a portion of the conductive layer such that undercut of the conductive layer under the photo resist layer is observed (col. 3, line 65 to col. 4, line 29 and FIG. 4); removing the photo resist layer; and implanting multiple (M) second ions into the polysilicon structure to form the lightly doped drain **34**, the step of implanting uses the undercut conductive layer as a third mask (col. 4, line 61 to col. 5, line .13 and FIG. 5).

In re claim 11, **You** discloses a method of forming a lightly doped drain, the lightly doped drain is formed in a thin film transistor, comprising: providing a glass substrate **10** and a polysilicon structure **13** on the glass substrate; depositing an insulating layer **15** on the polysilicon structure and the glass substrate; depositing a metal layer **17** on the insulating layer (col. 3, lines 34-64 and FIG. 2); forming a photo resist layer **21**; having a transferred, pattern on the metal layer; dry etching a portion of the metal layer to expose a portion of the insulating layer, the step of dry etching uses the photo resist layer as a first mask; implanting multiple (M) first ions into the polysilicon structure, the step

of implanting uses the photo resist layer and the metal layer as a second mask; isotropic etching a portion of the metal layer such that undercut of the metal layer under the photo resist layer is observed (col. 3, line 65 to col. 4, line 29 and FIG. 4), the step of isotropic etching including a step of wet etching (col.3, line 65 to col. 4, line 8); removing the photo resist layer; and implanting multiple (M) second ions into the polysilicon structure to form the lightly doped drain **34**, the step of implanting uses the undercut metal layer as a third mask (col. 4, line 61 to col. 5, line .13 and FIG. 5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (U.S. Patent 4,682,404) in view of You (U.S. Patent 6,806,036).

In re claims 2-5, **Miller** does not explicitly disclose that the semiconductor structure including a substrate and a polysilicon structure on the substrate, wherein the step of implanting the M first ions comprises implanting the M first ions into the polysilicon structure and the step of implanting the M second ions comprises implanting the M second ions into the polysilicon structure and wherein the conductive layer including a metal layer.

You, however, discloses that the semiconductor structure including a substrate **10** and a polysilicon structure **23** on the substrate, wherein the step of implanting the M first

ions comprises implanting the M first ions into the polysilicon structure and the step of implanting the M second ions comprises implanting the M second ions into the polysilicon structure (col. 4, line 21 to col. 5, line 4 and FIGS. 4-5) and wherein the conductive layer **17** or **27** including a metal layer (Al-contained metal layer and a Cr layer depending on circumstances) (col. 3, lines 48-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Miller and You to enable the semiconductor structure including a substrate and a polysilicon structure on the substrate of Miller to be formed and furthermore to provide a method for manufacturing polysilicon type thin film transistors that can reduce the number of the manufacturing process without causing a quality problem (col. 2, lines 7-10, You).

In re claim 7, **Miller** and **You** disclose that the step of forming the insulation layer comprises forming an oxide layer (col. 5, lines 15-28, Miller) (col. 3, lines 48-64, You) but does not explicitly disclose comprises forming an oxide layer and a silicon nitride layer on the oxide layer. However, the step of forming the insulating layer comprises forming an oxide layer and a silicon nitride layer on the oxide layer is well-known to one of ordinary skill in the art at the time of the invention was made.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
December 9th, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER